#2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Michael S. BERTONE et al.	§		
		§		
Serial No.:	09/651,924	§	Group Art Unit:	2154 ~~2151~~
		§		
Filed:	August 31, 2000	§	Examiner:	UNKNOWN
		§		
For:	Mechanism To Control The Allocation Of An N-Source Shared Buffer	§		

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Att'y. Docket No. 1662-31400
Client Docket No. P00-3212
Date: February 20, 2001

Sir:

This Information Disclosure Statement, including completed Form PTO-1449, comprises a list of pertinent art of which Applicants are aware. A copy of each publication listed on Form PTO-1449 is enclosed herewith.

Consideration of the following related co-pending applications is requested:

ATTORNEY DOCKET NO.	SERIAL NO.	FILING DATE	TITLE
1662-23700	09/653,642	08/31/00	Apparatus And Method For Interfacing A High Speed Scan-Path With Slow-Speed Test Equipment
1662-27300	09/652,322	08/31/00	Priority Rules For Reducing Network Message Routing Latency
1662-27400	09/652,703	08/31/00	Scalable Directory Based Cache Coherence Protocol
1662-27500	09/652,391	08/31/00	Scalable Efficient I/O Port Protocol
1662-27600	09/652,552	08/31/00	Efficient Translation Lookaside Buffer Miss Processing In Computer Systems With A Large Range Of Page Sizes
1662-27700	09/651,949	08/31/00	Fault Containment And Error Recovery Techniques In A Scalable Multiprocessor
1662-27800	09/652,834	08/31/00	Speculative Directory Writes in A Directory Based Cache Coherent Nonuniform Memory Access Protocol
1662-27900	09/652,314	08/31/00	Special Encoding Of Known Bad Data

ATTORNEY DOCKET NO.	SERIAL NO.	FILING DATE	TITLE
1662-28000	09/652,165	08/31/00	Broadcast Invalidate Scheme
1662-28100	09/652,704	08/31/00	Mechanism To Track All Open Pages In A DRAM Memory System
1662-28200	09/653,093	08/31/00	Programmable DRAM Address Mapping Mechanism
1662-29200	09/652,323	08/31/00	Computer Architecture And System For Efficient Management Of Bi-Directional Bus
1662-29300	09/652,452	08/31/00	An Efficient Address Interleaving With Simultaneous Multiple Locality Options
1662-29400	09/653,092	08/31/00	A High Performance Way Allocation Strategy For A Multi-Way Associative Cache System
1662-29500	09/651,948	08/31/00	Method And System For Absorbing Defects In High Performance Microprocessor With A Large N-Way Set Associative Cache
1662-29600	09/652,324	08/31/00	A Method For Reducing Directory Writes And Latency In A High Performance, Directory-Based, Coherency Protocol
1662-30800	09/653,094	08/31/00	Mechanism To Reorder Memory Read And Write Transactions For Reduced Latency And Increased Bandwidth
1662-30900	09/652,325	08/31/00	System For Minimizing Memory Bank Conflicts In A Computer System
1662-31000	09/651,945	08/31/00	Computer Resource Management And Allocation System
1662-31100	09/653,643	08/31/00	Input Data Recovery Scheme
1662-31200	09/652,451	08/31/00	Fast Lane Prefetching
1662-31300	09/652,480	08/31/00	Mechanism For Synchronizing Multiple Skewed Source-Synchronous Data Channels With Automatic Initialization Feature
1662-31500	09/652,315	08/31/00	Chaining Directory Reads And Writes To Reduce DRAM Bandwidth In A Directory Based CC-NUMA Protocol

The submission of this Information Disclosure Statement and the references submitted therewith is not an admission that the art cited is "prior" with respect to the present invention, nor is it a representation, that no better art exists. Applicants hereby reserve the right to swear behind

FORM PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary) (37 CFR 1.98(b))	ATTY. DOCKET NO. 1662-31400 (P00-3212)	SERIAL NO. 09/651,814
	APPLICANTS Michael S. BERTONE et al.	
	FILING DATE August 31, 2000	GROUP ~~2151~~ 2654

U. S. PATENT DOCUMENTS

Examiner Initial		Patent Number	Issue Date	Patentee	Class	Sub-class	Filing Date (If Appropriate)
DW	AA	5261066	11/09/93	Jouppi et al.	395	425	03/27/90
	AB	5317718	05/31/94	Jouppi	395	425	01/25/93
	AC	5758183	05/26/98	Scales	395	825	07/17/96
	AD	5761729	06/02/98	Scales	711	148	07/17/96
	AE	5787480	07/28/98	Scales et al.	711	148	07/17/96
	AF	5802585	09/01/98	Scales et al.	711	154	07/17/96
	AG	5809450	09/15/98	Chrysos et al.	702	186	11/26/97
	AH	5875351	02/23/99	Mick	365	233	05/28/97
	AI	5890201	03/30/99	McLellan et al.	711	108	07/01/97
	AJ	5893931	04/13/99	Peng et al.	711	206	01/15/97
	AK	5918249	06/29/99	Hammond	711	205	05/05/95
	AL	5918251	06/29/99	Yamada et al.	711	207	12/23/96
	AM	5920713	07/13/99	Chrysos et al.	395	591	11/26/97
	AN	5958027	09/07/99	Scales et al.	711	148	02/03/97
	AO	5968135	10/12/99	Anderson et al.	712	219	11/26/97
	AP	5978874	11/09/99	Lewchuk	711	137	12/09/97
	AQ	6000044	12/07/99	Chrysos et al.	714	47	11/26/97
	AR	6070227	05/30/2000	Rokicki	711	117	10/31/97
DW	AS	6085295	07/04/2000	Sunaga et al.	711	168	09/19/97

FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION

		Document Number	Publication Date	Country or Patent Office	Class	Sub-Class	Translation	
							Yes	No

FORM PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO. 1662-31400 (P00-3212)	SERIAL NO. 09/651,924
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	APPLICANTS Michael S. BERTONE et al.	
(Use several sheets if necessary) (37 CFR 1.98(b))	FILING DATE August 31, 2000	GROUP ~~2151~~ 2154

OTHER DOCUMENTS (Including Author, Title, Date, Relevant Pages, Place of Publication)			
		AT	*Alpha Architecture Reference Manual*, Third Edition, The Alpha Architecture Committee, 1998 Digital Equipment Corporation (21 p.), in particular pages 3-1 through 3-15
		AU	~~*A Logic Design Structure For LSI Testability*, E. B. Eichelberger et al., 1977 IEEE (Pages 462-468)~~
		AV	~~*Direct RDRAM™ 256/288-Mbit (512Kx16/18x32s)*, Preliminary Information Document DL0060 Version 1.01 (69 p.)~~
		AW	~~*Testability Features of AMD-K6™ Microprocessor*, R. S. Fetherston et al., Advanced Micro Devices (8 p.)~~
		AX	*Hardware Fault Containment in Scalable Shared-Memory Multiprocessors*, D. Teodosiu et al., Computer Systems Laboratory, Stanford University (12 p.), 1977
		AY	~~*Cellular Disco: resource management using virtual clusters on shared-memory multiprocessors*, K. Govil et al., 1999 ACM 1-58113-140-2/99/0012 (16 p.)~~
DN		AZ	*Are Your PLDs Metastable?*, Cypress Semiconductor Corporation, March 6, 1997 (19 p.)
		BA	~~*Rambus® RIMM™ Module (with 128/144Mb RDRAMs)*, Preliminary Information, Document DL0084 Version 1.1 (12 p.)~~
		BB	~~*Direct Rambus™ RIMM™ Module Specification Version 1.0*, Rambus Inc., SL-0006-100 (32 p.), 2000~~
DN		BC	*End-To-End Fault Containment In Scalable Shared-Memory Multiprocessors*, D. Teodosiu, July 2000 (148 p.)
Examiner [signature]			Date Considered 11/10/06

EXAMINER: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.